CLAIMS

What is claimed is:

1. A method comprising:

allocating memory non-uniformly between a plurality of memory channels associated with a network processor;

determining a selected memory channel from said plurality of memory channels for a program address; and

mapping said program address to a physical address within said selected memory channel.

2. The method of claim 1 further comprising interleaving all of said memory in memory channels having a same amount of memory with a same amount of memory in the memory channel having the non-uniform amount of memory.

3. The method of claim 1 wherein said determining a selected memory channel comprises:

determining whether the program address accesses an interleaved portion of memory and when said program memory address does access an interleaved portion of memory then performing an operation on said program address to obtain a memory channel number and when said program memory address does not access an interleaved portion of memory then selecting the memory channel containing non-interleaved memory.

4. The method of claim 1 wherein said mapping said program address to a physical address comprises:

determining whether the program address accesses an interleaved portion of memory and when said program memory address does access the interleaved portion of memory then performing address interleaving of said program address and when said program memory address does not access the interleaved portion of memory then subtracting a predetermined value from said program address to obtain a physical address in the selected memory channel.

5. The method of claim 2 wherein said interleaving comprises:

determining the number of consecutive bits of a predetermined portion of the program address bits that are ones;

right shifting program address bits by a predetermined number of bits to obtain a shifted address;

adding a predetermined offset value to the shifted address to obtain an interim physical address; and

appending a predetermined number of program address bits to said interim physical address to obtain a physical address within said selected memory channel.

6. The method of claim 1 wherein said allocating memory non-uniformly comprises allocating twice as much memory to a first memory channel than is allocated to other memory channels.

7. The method of claim 1 wherein said allocating memory non-uniformly between a plurality of memory channels comprises allocating memory non-uniformly between a first memory channel (channel 0), a second memory channel (channel 1) and a third memory channel (channel 2).

8. The method of claim 3 wherein said determining whether the program address accesses an interleaved portion of memory comprises determining whether the program address accesses a lower three/fourths of memory.

9. The method of claim 3 wherein said performing an operation on said program address comprises performing summing modulo three arithmetic on at least a portion of said program address to obtain a remainder, said remainder comprising the memory channel number

10. A system comprising

a network processor; and

a plurality of memory channels in communication with said network processor, wherein at least one of said memory channels has more memory than another of said memory channels.

11. The system of claim 10 wherein all of said memory in memory channels having a same amount of memory and a same amount of memory in the memory channel having the non-uniform amount of memory are interleaved.

12. The system of claim 10 wherein said network processor determines a memory channel for a memory access by determining whether said memory access is to an interleaved portion of memory and if the access is to an interleaved portion then performing an operation on said program address and when said program memory address does not access an interleaved portion of memory then selecting the memory channel containing non-interleaved memory.

13. The system of claim 10 wherein said network processor maps said program address to a physical address by determining whether the program address accesses an interleaved portion of memory and when said program memory address does access the interleaved portion of memory then performing address interleaving of said program address and when said program memory address does not access the interleaved portion of memory then subtracting a predetermined value from said program address to obtain a physical address in the selected memory channel.

14. An article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

allocating memory non-uniformly between a plurality of memory channels;

determining a selected memory channel from said plurality of memory channels for a program address; and

mapping said program address to a physical address within said selected memory channel.

15. The article of claim 14 further comprising instructions that when executed by a machine result in interleaving all of said memory in memory channels having a same amount of memory with a same amount of memory in the memory channel having the non-uniform amount of memory.

16. The article of claim 14 wherein said determining a selected memory channel comprises:

determining whether the program address accesses an interleaved portion of memory and when said program memory address does access an interleaved portion of memory then performing an operation on said program address to obtain a memory channel number and when said program memory address does not access an interleaved portion of memory then selecting the memory channel containing non-interleaved memory.

17. The article of claim 14 wherein said mapping said program address to a physical address comprises:

determining whether the program address accesses an interleaved portion of memory and when said program memory address does access the interleaved portion of memory then performing address interleaving of said program address and when said program memory address does not access the interleaved portion of memory then subtracting a predetermined value from said program address to obtain a physical address in the selected memory channel.

18. A method comprising:

designating a range of addresses defined as the memory between an upper address to perform range checking and a lower address to perform range checking;

monitoring memory accesses; and

determining if any of said memory accesses occur within said range of addresses and in response to a memory access occurring with said range of memory addresses then performing a predetermined operation.

19. The method of claim 18 wherein said performing a predetermined operation comprises performing an operation selected from the group consisting of interrupting the core processor, aborting the pending memory operation, executing a halt, and sending an exception.

20. The method of claim 18 wherein said determining if any of said memory accesses occur within said range of addresses comprises determining at least one of the group consisting of determining if the starting address of the memory access lies between said upper address and said lower address, determining if the ending address of the memory access lies between said upper address and said lower address, and determining if the lower address lies between the starting address of the memory access and the ending address of the memory access.

21. The method of claim 18 wherein said upper address and said lower address are located in different blocks of memory.

22. The method of claim 18 wherein said starting address of a memory access and an ending address of the memory access are located in different blocks of memory.

23. An article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

designating a range of addresses defined as the memory between an upper address to perform range checking and a lower address to perform range checking; and

monitoring memory accesses and determining if any of said memory accesses occur within said range of addresses and in response to a memory access occurring with said range of memory addresses then performing a predetermined operation.

24. The article of claim 23 wherein said performing a predetermined operation comprises performing an operation selected from the group consisting of interrupting the core processor, aborting the pending memory operation, executing a halt, and sending an exception.

25. The article of claim 23 wherein said determining if any of said memory accesses occur within said range of addresses comprises determining at least one of the group consisting of determining if the starting address of the memory access lies between said upper address and said lower address, determining if the ending address of the memory access lies between said upper address and said lower address, and determining if the lower address lies between the starting address of the memory access and the ending address of the memory access.

26. The article of claim 23 wherein said upper address and said lower address are located in different blocks of memory.

27. The article of claim 23 wherein said starting address of a memory access and an ending address of the memory access are located in different blocks of memory.